

REMARKS

Claims 22-59, 3, 9 and 18

Initially, Applicant notes that Claims 22-59 are not rejected under 35 USC §103. Accordingly, it is believed that these claims are allowable, except the double patenting rejection, and once the double patenting rejection has been overcome, these claims will be allowed. Also, previously, Claims 3, 9 and 18 were objected to as being dependent on a rejected base claim but would be allowable if rewritten in independent form. Since these claims have also not been rejected under 35 USC §103, it is believed that once the double patenting rejection has been overcome, these claims will again have allowable subject matter.

Amendments to Claims

Except as discussed below, Applicant is amending the claims to correct informalities therein. These amendments are not in response to a patentability rejection.

Applicant will now address each of the Examiner's rejections in the order in which they appear in the Office Action.

Double Patenting

In the Office Action, the Examiner rejects Claims 1-67 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-49 of U.S. Patent no. 6,548,960. As Applicant is still trying to overcome the §103 rejections and the claims may not be in their final form, it is requested that this rejection be held in abeyance until the other rejections have been overcome.

Claim Rejections - 35 USC §103

Claims 1-2, 4, 7-8, 10, 13-15, 17 and 19

The Examiner rejects Claims 1-2, 4, 7-8, 10, 13-15, 17 and 19 under 35 USC §103(a) as being unpatentable over Yamada et al. (US 5,990,629) in view of Sano (US 6,246,384). This rejection is respectfully traversed.

More specifically, independent Claim 1 recites that the eliminating TFT is controlled by the second gate signal line driver circuit.

The Examiner admits that Yamada does not disclose this feature. However, the Examiner contends that Sano teaches an eliminating TFT for controlling EL driving TFT, controlled by second driver. The Examiner then contends that it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Sano in the Yamada system in order to enable the current supply to the EL device to be controlled. Applicant respectfully disagrees.

First, Applicant respectfully submits that neither of the cited references discloses an eliminating TFT controlled by the second gate signal line driver circuit, as recited in independent Claim 1 of the present application.

Further, the Examiner's modification of Yamada with Sano to arrive at the claimed invention is improper. As is well established law, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. See e.g. MPEP §2143.01.

No such teaching, suggestion or motivation is present here, and the Examiner's explanation of such is insufficient. For example, in support of the modification, the Examiner cites col. 2, lns. 35-40 in Sano. However, this section merely states that an object of the invention of Sano is "to easily enable the current supply to the EL device to be controlled." This

statement is not directed to TFT 56 (the alleged eliminating TFT), but to the invention of the patent as a whole. Hence, this citation provides insufficient motivation to combine the references or to modify Yamada with Sano.

Further, where would one skilled in the art insert this alleged eliminating TFT from Sano in the circuit of Yamada? Which circuit in Yamada would be modified? Why and how? There appears to be no teaching, suggestion or motivation for where the alleged eliminated TFT can be inserted, as required by MPEP §2143.01.

Therefore, as no such teaching, suggestion or motivation exists with regard to this rejection, no prima facie case has been established, and the rejection of independent Claim 1 should be reversed.

Independent Claims 7 and 13 (and 22, 30, 41 and 49) recite electrical connections between the first to third TFTs, the source signal lines, the second gate signal lines, and the power supply lines. It is respectfully submitted that neither cited reference, either individually or combined (which Applicant does not admit is proper), shows these electrical connections.

Accordingly, these independent claims and the claims dependent thereon are patentable over the cited references, and it is respectfully requested that this rejection be withdrawn.

Claims 5, 11 and 20

The Examiner also rejects Claims 5, 11 and 20 under 35 USC §103(a) as being unpatentable over Yamada et al. and Sato [sic Sano] and further in view of Chiu (US 5,606,348). This rejection is also respectfully traversed.

Each of these claims is a dependent claim. Therefore, for at least the reasons discussed above for the independent claims, these claims are also patentable over the cited references, and it is respectfully requested that this rejection be withdrawn.

Claims 6, 12 and 21

The Examiner also rejects Claims 6, 12 and 21 under 35 USC §103(a) as being unpatentable over Yamada et al. and Sato [sic Sano] and further in view of Okayama et al. (US 5,899,575). This rejection is also respectfully traversed.

Each of these claims is a dependent claim. Therefore, for at least the reasons discussed above for the independent claims, these claims are also patentable over the cited references, and it is respectfully requested that this rejection be withdrawn.

Claim 16

The Examiner also rejects Claim 16 under 35 USC §103(a) as being unpatentable over Yamada et al. and Sato [sic Sano] and further in view of Hsieh (US 5,876,865). This rejection is also respectfully traversed.

This claim is a dependent claim. Therefore, for at least the reasons discussed above for the independent claims, this claim is also patentable over the cited references, and it is respectfully requested that this rejection be withdrawn.

Claims 60-61, 64-65

The Examiner also rejects Claims 60-61, 64-65 under 35 USC §103(a) as being unpatentable over Osada et al. in view of Yamada et al. and Sato [sic Sano]. This rejection is also respectfully traversed.

In the Office Action, the Examiner contends that the data electrode driver IC (reference numeral 4), the scanning electrode driver IC (reference numeral 2), the scanning electrode driver IC (reference numeral 3) of Fig. 1 in Osada correspond to the source signal line driver circuit, the

first gate signal line driver circuit, and the second gate signal line driver circuit of the claimed invention, respectively. Applicant respectfully disagrees.

The cited driver ICs of Osada are for driving the scanning electrodes and the data electrodes constituting the EL elements, not for driving “gate signal lines” or “source signal lines” electrically connected to transistors in pixels, as in the claimed invention. More specifically, one skilled in the art would recognize that in general, gate signal lines are for providing signals (electric potentials) to the *gates of transistors* while source signal lines are for providing signals to *sources or drains of transistors*. Hence, the driver ICs of Osada are different than the claimed elements.

Further, none of the cited references disclose or suggest the feature of “at least one of the pixels comprises at least a first TFT electrically connected to the first gate signal line driver circuit, and a second TFT electrically connected to the second gate signal line driver circuit,” as recited in independent Claims 60 and 64. The Examiner appears to merely contend that Sano shows an eliminating TFT and that is sufficient. Sano, however, does not disclose or suggest two TFTs in a pixel electrically connected to different gate signal line driver circuits, as required in Claims 60 and 64.

Accordingly, it is respectfully submitted that independent Claims 60 and 64 and those claims dependent thereon are patentable over the cited references, and it is requested that this rejection be withdrawn.

Claims 62 and 66

Claims 62 and 66 are rejected under 35 USC §103(a) as being unpatentable over Yamada et al. and Osada et al., Sano, and further in view of Chiu. This rejection is also respectfully traversed.

Each of these claims is a dependent claim. Therefore, for at least the reasons discussed above for the independent claims, these claims are also patentable over the cited references, and it is respectfully requested that this rejection be withdrawn.

Claims 63 and 67

Claims 63 and 67 are rejected under 35 USC §103(a) as being unpatentable over Yamada et al. and Osada et al., Sano and further in view of Okayama et al. This rejection is also respectfully traversed.

Each of these claims is a dependent claim. Therefore, for at least the reasons discussed above for the independent claims, these claims are also patentable over the cited references, and it is respectfully requested that this rejection be withdrawn.

Therefore, it is respectfully submitted that all of the rejections under §103 has been overcome, and it is requested that these rejections be withdrawn.

New Claims

Applicant is adding new Claims 68-78. Each of these claims is a dependent claim, and each is allowable for at least the reasons discussed above for the independent claims. Accordingly, it is respectfully requested that these new claims be entered and allowed.

Please charge our deposit account 50/1039 for any fee due for these new claims.

Information Disclosure Statement

Applicant is submitting an information disclosure statement (IDS) herewith. It is respectfully requested that this IDS be entered and considered prior to the issuance of any further action for this application.


Conclusion

Therefore, it is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any fee is due for this amendment, please charge our deposit account 50/1039.

Favorable consideration is earnestly solicited.

Respectfully submitted,

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